17CS34 COMPUTER ORGANIZATION

Question Bank:

# INPUT/OUTPUTORGANIZATION

1. Explain the architecture and addressing scheme of USB [l2][co3]
2. Describe how a read operation is performed on a PCI bus [l1][co3]
3. Define bus arbitration? Explain different approaches to bus arbitration [l1][l2][co3]
4. a) Define memory mapped I/O and I/O mapped I/O with examples [l1] [co3]

b)Define the terms ‘cycle stealing and ‘block mode’ [l1] [co3]

1. List the SCSI bus signals with their functionalities [l1] [co3]
2. Explain: i) Synchronous bus ii) Asynchronous bus [l2] [co3]

# MEMORYSYSTEM

# Explain the internal organisation of a 16 Megabits DRAM chip configured as 2MX8 cells [l2] [co4]

# With a block diagram, explain the direct and set associative mapping between cache and main memory [l2] [co4]

# Briefly explain any four non-volatile memory concepts [l2] [co4]

# Describe the memory hierarchy with respect to speed, size and cost along with neat sketch [l1] [co4]

# Briefly explain any two cache mapping functions [l2] [co4]

# Define is virtual memory? With a diagram, explain how virtual memory address is translated [l1] [l2] [co4]

# With a neat diagram, explain the translation of a virtual address to a physical address [l2] [co4]

# a) Describe the principles of magnetic disk [l1] [co4]

# b) Explain direct memory mapping technique [l2] [co4]

# Draw for lK x 1memory chip with neat figure [l1] [co4]

# Discuss in detail any one feature of memory design that leads to improved performance of computer [l2] [co4]

# BASICPROCESSINGUNIT

* 1. List out the actions needed to execute the instruction ADD (R3), R1. Write and explain the sequence of control steps for the execution of the same [l1] [co5]
  2. With a neat block diagram, explain hardwired control unit. Show the generation Zin and end control signals. [l1] [co5]
  3. Explain the control sequence for execution of an unconditional branch instruction. [l2] [co5]
  4. Explain multiple bus organization and its advantages with neat sketch [l2] [co5]
  5. List out the control sequence for the instruction ADD R4, R5, R6 for three bus organisation. [l1] [co5]
  6. With a neat sketch, explain the organisation of a micro programmed control unit [l2] [co5]
  7. With an example, explain the field coded micro instructions [l2] [co5]
  8. With neat sketch explain the single-bus organization of the data path inside a processor [l2] [co5]
  9. Define the control sequence for an un-conditional branch instruction [l1] [co5]
  10. Draw the block diagram of the control unit organization and describe in brief [l1] [l1] [co5]

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